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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,608	10/20/2003	Dureseti Chidambarrao	FIS920030244US1	2585

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,608	CHIDAMBARRAO ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 5/18/05. Currently, claims 1-22 and 27 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4, 6,7, 9, 10, 12, 16, 17, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Kubo et al. US Patent 6,6399,970.

Kubo discloses the semiconductor method as claimed. See figures 1-16, and corresponding text, where Kubo teaches, pertaining to claims 1 and 16, a method of manufacturing a semiconductor structure, comprising the steps of: forming a p-type field-effect-transistor (pFET) channel **17p/15p/14p** and a n-type field-effect-transistor (nFET) channel **17n/15n/14n** in a substrate **10** (figure 1; col. 8, lines 37-41 n-channel; col. 11, lines 55-59, p-channel); providing a first layer of material **15p** within the pFET channel having a lattice constant different than the lattice constant of the substrate, the second layer of material being different from the first layer of material (figures 1 and 3-6; col. 9, lines 15-38; col. 11, lines 6-59); providing a second layer **14n** of material within the nFET channel having a lattice constant different than the lattice constant of the substrate figures 1 and 3-6; col. 8, lines 60-67; col. 10, lines 10-57, ***Note***: that the lattice constant is different for the nFET channel and the pFET

channel as evidence by the tensile and compressive stress relative to the substrate, provided in the pFET and nFET device layers); forming an epitaxial semiconductor layer **17n/17p** over the first layer of material in the pFET channel and the second layer of material in the nFET channel, the epitaxial semiconductor layer having substantially a same lattice constant as the substrate such that a stress component is created within the pFET channel and the nFET channel, or creating a stress component opposite to that of the first layer of material within the pFET channel and the second layer of material within the nFET channel (claim 16; col. 10, lines 22-30 and 45-57; Si, as is the substrate, has substantially the same lattice constant; col. 12, lines 35-49, epitaxially grown; col. 11, lines 15-22; col. 8, lines 30-35).

Pertaining to claims 2 and 17, Kubo teaches, the method, wherein the pFET channel and the nFET channel are formed simultaneously (col. 9, lines 50-55).

Pertaining to claim 4, Kubo teaches, wherein the first layer of material is SiGe having a content of Ge approximately greater than 25% in ratio to Si (col. 8, lines 46-50).

Pertaining to claim 6, Kubo teaches, the method wherein, the second layer of material is SiGe (figure 1; col. 9, lines 25-30).

Pertaining to claim 7, Kubo teaches, the method, wherein the first layer of material is SiGe having a constant of Ge approximately greater than 25% in ratio to Si (figure 1; col. 9, lines 25-30).

Pertaining to claims 9 and 21, Kubo teaches, the method further comprising the steps of: forming a gate oxide structure **19n/19p** over the epitaxial semiconductor layer (col. 9, lines 40-45); and forming extensions and a drain region and source region in an Si layer of the substrate on sides of gate oxide structure (figure 1; col. 9, lines 1-15 and 40-45).

Pertaining to claim 10, the method, wherein the forming of the nFET and pFET channels includes etching an Si layer of the substrate to approximately a depth of about 200 to 400 (col. 9, lines 60-65, ***Note***: the total thickness of the layers within the nFET and pFET channels ranges to approximately about 65 to 600).

Pertaining to claim 12, Kubo teaches the method wherein, further comprising forming shallow trench structures **20** within the substrate (figure 1; col. 9, lines 45-50).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 11, 18 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo et al. US Patent 6,399,970 in view of Vossenberg et al. US Patent 6,790,699.

Kubo discloses the semiconductor method substantially as claimed. See the preceding rejection of claims 1, 2, 4, 6, 7, 9, 10, 12, 16, 17, and 21 under 35 U.S.C. 102(b).

However, Kubo fails to show, pertaining to claims 3 and 18, wherein the pFET channel and the nFET channel are formed separately. In addition, pertaining to claims 11 and 22, the method wherein: the first layer of material is formed by placing a hard mask over the nFET channel and growing the first layer of material within the pFET channel; and the second layer of material is formed by placing a hard mask over the pFET channel and growing the second layer of material within the nFET channel.

Vossenberg teaches, in figures 7A-7C, and corresponding text, a patterned isolation layer having exposed regions of the monocrystalline layer and, epitaxially growing through the exposed regions (col. 4, lines 23-28; col. 6, lines 1-18).

Therefore, It would be obvious to one of ordinary skill in the art to include forming the pFET channel and the nFET channel separately, pertaining to claims 3 and 18, in the method of Kubo, based on the both the teachings of Kubo in view of Vossenberg, with the motivation, that Kubo teaches in the end result, that both channels (pFET and nFET) are provided, therefore, the method of forming these channels, either sequentially or separately, would prove to be insignificant since both methods would result in the formation of the pFET and nFET channels. In addition, both methods of formation would result in the same device.

In addition, it would have been obvious to one of ordinary skill in the art to, substitute, the method wherein: the first layer of material is formed by placing a hard mask over the nFET channel and growing the first layer of material within the pFET channel; and the second layer of material is formed by placing a hard mask over the pFET channel and growing the second layer of material within the nFET channel, pertaining to claims 11 and 22, respectively, in the method of Kubo, according to the teachings of Vossenberg, with the motivation that, the epitaxial layer taught in Vossenberg, is formed of the silicon layer through the exposed regions of the isolation layer. Therefore, it would be obvious to one of ordinary skill the art to use a hard mask such as, an insulating layer, for the purpose of epitaxially growing a layer within the desired regions of the pFET and nFET channels from the silicon layer.

Claims 5, 13, and 15, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo et al. US Patent 6,399,970.

Kubo discloses the semiconductor method substantially as claimed. See the preceding rejection of claims 1, 2, 4, 6, 7, 9, 10, 12, 16, 17, and 21 under 35 U.S.C. 102(b).

However, Kubo fails to show, pertaining to claim 5, the method wherein the first layer of material creates a tensile stress within the epitaxial semiconductor layer of greater than 3Gpa. In addition, Kubo fails to show, pertaining to claim 13, the method, wherein the first layer of material and the second layer of material are grown to a height about 100 to 300 . Finally, Kubo fails to show, pertaining to claim 15, the method, wherein the first layer of material and the second layer of material are both SiGe material, having a larger Ge percentage than approximately 25% to 30% to apply for the pFET.

Kubo teaches, in prior art figures 15, and 16, and corresponding text, pertaining to claim 5, a method wherein the first layer of material creates a tensile stress within the epitaxial semiconductor layer (col. 1, lines 20-35 and 45-57; col. 2, lines 10-25). In addition, Kubo teaches, pertaining to claim 13, the method, wherein the first layer of material and the second layer of material are grown to a height about 3 to 5 nm converted to 30-50 . Finally, Kubo teaches, pertaining to claim 15, that the first and second layers are formed of SiGe and, that the composition of SiGe can be controlled by adjusting the composition of this material. (col. 1, lines 25-35 and lines 45-57; col. 2, lines 10-25; col. 9, lines 60-67, respectively)

Therefore, it would have been obvious to one of ordinary skill in the art to, incorporate, the method wherein the first layer of material creates a tensile stress within the epitaxial semiconductor layer of greater than 3Gpa; the method, wherein the first layer of material and the

second layer of material are grown to a height about 100 to 300 ; the method, wherein the first layer of material and the second layer of material are both SiGe material, having a larger Ge percentage than approximately 25% to 30% to apply for the pFET, pertaining to claims 5, 13 and 15, respectively, in the method of Kubo, according to the teachings of Kubo, with the motivation that, the prior art, taught by Kubo, teaches that the composition of the Si/SiGe can be controlled to have the desired amount of strain and band gap. For example, for forming an n-channel layer having a tensile strain, the Ge composition rate in the SiGe buffer layer 102 is gradually changed. Therefore it would have been obvious to have an epitaxial semiconductor layer with a first layer creating a tensile stress greater than 3Gpa, for the purpose of forming an n-channel layer by creating a tensile strain within the transistor device, where a tensile stress greater than 3Gpa would result in routine experimentation. It would have been obvious to have the first layer of material and the second layer of material to be grown to a height about 100 to 300 , with the motivation that, since Kubo teaches, the first and second material layers to have a thickness of 30-50 , the claimed height of the first and second layers of material are considered to be within conventional specifications, where the heights are formed within the same order. Finally, it would be obvious to have the first layer of material and the second layer of material both be made of SiGe material, having a larger Ge percentage than approximately 25% to 30% be applied to the pFET, with the motivation that, since Kubo teaches, that both the first and second material layers are made of SiGe, in addition, the composition of the Si/SiGe can be controlled to have a desired amount of strain and band gap. Therefore, it would be obvious to one of ordinary skill in the art to adjust the Ge composition rate to the other layer for the purpose of creating a p-

channel layer for the pFET device, furthermore, would be routine experimentation since the p-channel layer may be formed by changing the Ge composition rate.

Claims 8, 19, 20 and 27, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo el al. US Patent 6,399,970 in view of Candelaria US Patent 5,683,934.

Kubo discloses the semiconductor method substantially as claimed. See the preceding rejection of claims 1, 2, 4, 6, 7, 9, 10, 12, 16, 17, and 21 under 35 U.S.C. 102(b). In addition, Kubo shows, pertaining to claim 19, the second layer of material is SiGe. Also, Kubo shows, pertaining to claim 20, the method wherein: the first layer of material creates a compressive stress within the epitaxial semiconductor layer within the pFET channel; and the second layer of material creates a tensile stress within the epitaxial semiconductor layer within the nFET channel. Kubo shows, pertaining to claim 27, a method of manufacturing a semiconductor structure, comprising the steps of: forming a p-type field-effect-transistor (pFET) channel **17p/15p/14p** and a n-type field-effect-transistor (nFET) channel **17n/15n/14n** in a substrate **10** (figure 1; col. 8, lines 37-41 n-channel; col. 11, lines 55-59, p-channel); providing a layer **15p** within the pFET channel having a lattice constant different than the lattice constant of the substrate (figures 1 and 3-6; col. 9, lines 15-38; col. 11, lines 6-59); providing a layer **15n** within the nFET channel having a lattice constant different than the lattice constant of the substrate figures 1 and 3-6; col. 8, lines 60-67; col. 10, lines 10-57, ***Note***: that the lattice constant is different for the nFET channel and the pFET channel as evidence by the tensile and compressive stress relative to the substrate, provided in the pFET and nFET device layers); forming an epitaxial semiconductor layer **17n/17p** over the layers in the pFET channel and the second layer

of material in the nFET channel, the epitaxial semiconductor layer having substantially a same lattice constant as the substrate such that a stress component is created within the pFET channel and the nFET channel, or creating a stress component opposite to that of the first layer of material within the pFET channel and the second layer of material within the nFET channel (claim 16; col. 10, lines 22-30 and 45-57; Si, as is the substrate, has substantially the same lattice constant; col. 12, lines 35-49, epitaxially grown; col. 11, lines 15-22).

However, Kubo fails to show, pertaining to claim 8, 19 and 27, the method, wherein the first layer of material is Si:C.

Candelaria teaches, in figures 1-5, and corresponding text, the use of a carbon-doped silicon channel within a complementary p-channel MOSFET device. (col. 3, lines 32-61).

Therefore, it would have been obvious to one of ordinary skill in the art to substitute in the method of Kubo, pertaining to claims 8 and 19, wherein the first layer of material is Si:C and the second layer of material is SiGe, in the method of Kubo, according to the teachings of Candelaria, with the motivation that, the there is a relative size difference between the carbon and germanium atoms where one of ordinary skill in the art would use a sufficiently lower amount of carbon atoms verse the germanium atoms to form a channel layer under tensile stress. In addition, it would be desirable to one of ordinary skill in the art to use the carbon-doped silicon channel layer, taught by Candelaria, with the motivation of enhancing the electron mobility, a reduction of surface scattering, hot carrier degradation, and noise effects.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo et al. US Patent 6,399,970 in view of Stanley Wolf and Richard N. Tauber, Silicon Processing For the VLSI Era, Vol. I, Second Edition, Lattice Press, 2000, pages 256-257.

Kubo discloses the semiconductor method substantially as claimed. See the preceding rejection of claims 1, 2, 4, 6, 7, 9, 10, 12, 16, 17, and 21 under 35 U.S.C. 102(b).

However, Kubo fails to show, pertaining to claim 14, wherein the substrate layer of a silicon on insulator.

Wolf teaches, the conventional advantages of forming a device on a silicon on insulator substrate (pages 256-257).

Therefore, it would have been obvious to one of ordinary skill in the art to, incorporate the substrate layer being silicon on insulator, in the method of Kubo, according to the teachings of Wolf, with the motivation that, Wolf teaches that SOI substrates are conventionally well known for their reduced parasitic capacitance, resulting in the creation of faster device. As a result, it would be more desirable to one of ordinary skill in the art to use of an SOI substrate, for the purpose of creating faster and more reliable semiconductor devices.

Response to Arguments

Applicant's arguments filed 5/16/05 have been fully considered but they are not persuasive. In the Applicant's Remarks on pages, 9-19:

The Applicant raises the clear issue of whether Kubo alone or in combination thereof, suggests a first layer of material within the pFET channel having a lattice constant different than the lattice constant of the substrate, a second layer of material within the nFET channel having a

lattice constant different than the lattice constant of the substrate, **the second layer of the material being different from the first layer of material** (with emphasis), or an epitaxial semiconductor layer having substantially a same lattice constant as the substrate that create stress components or opposite stress components.

The Examiner takes the position that Kubo alone and/or in combination thereof, does teach a second layer of material within the nFET channel being different from the first layer of material in addition, an epitaxial semiconductor layer having substantially a same lattice constant as the substrate that create stress components or opposite stress components. Specifically, Kubo teaches in figure 1, and corresponding text, a first layer SiGe **15p** within the PMOS channel region and a second layer SiGeC **14n** within the NMOS transistor region that is different from the first layer of material (col. 8, lines 37-41 n-channel; col. 11, lines 55-59, p-channel). In addition, Kubo teaches the formation of a tensile stress within the NMOS transistor channel, the formation of a compressive strain formed within the PMOS transistor channel, and forming an epitaxial layer over these layers, just as the Applicant describes with regards to the formation of opposite stress components formed within these channels (col. 11 lines 23-40; col. 13, lines 27-55). Therefore, forming an epitaxial semiconductor layer having the same lattice constant as the substrate must be obtained, due to the formation of opposite stress components formed within the different device channels.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
August 21, 2005

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